## Inhomogeneous hysteresis in local STM tunnel conductance with gate voltage in single layer MoS<sub>2</sub> on SiO<sub>2</sub>

Anjan Kumar Gupta Physics Department Indian Institute of Technology, Kanpur

Charge traps at the  $MoS_2/SiO_2$  interface result in non-ideal transport behavior, including hysteresis in  $MoS_2$  on  $SiO_2$  FETs. Our room temperature STM/S measurements in vacuum on atomically resolved single and few-layer  $MoS_2$  on  $SiO_2$  show n-doped behavior with the expected band gap close to 2.0 and 1.4 eV, respectively. The local tunnel conductance with gate-voltage Vg sweep exhibits a turn-on or off at a threshold Vg. This threshold value is found to depend on Vg sweep direction amounting to local hysteresis. This hysteresis is, expectedly, found to depend on both the extent and rate of Vg-sweep. Further, the spatial variation in the local threshold Vg value and the detailed conductance Vs Vg behavior indicate inhomogenieties in both the traps' density and their energy distribution. Further, while most of the single layer  $MoS_2$  was found to be n-doped, some rare locations exhibit a p-doping with both p and n-type Vg-thresholds in local conductance and an unusual hysteresis.